AMENDMENT TO THE CLAIMS

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1. (Currently Amended) A memory module comprising:

a printed circuit board having a first lateral portion and a second lateral portion;

a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;

a control logic bus connected to the plurality of identical integrated circuits, the control logic bus comprising a first set of address signal paths and a second set of address signal paths; and

a first register and a second register connected to the control logic bus, the first register accessing a first range and a second range of data bits, the second register accessing a third range and a fourth range of data bits, the first range and the second range of data bits being first and second non-contiguous subsets of a data word, and the third range and the fourth range of data bits being third and fourth non-contiguous subsets of the data word, wherein the first set of address signal paths connect the first register to the integrated circuits of the first row and the second row on the first lateral portion and the second set of address signal paths connect the second register to the integrated circuits of the first row and the second row on the second lateral portion.

2. (Original) The memory module of Claim 1, wherein:

the first range of data bits comprise data bits 0 to 15;

the second range of data bits comprise data bits 32 to 47;

the third range of data bits comprise data bits 16 to 31; and

the fourth range of data bits comprise data bits 48 to 63.

3. (Original) The memory module of Claim 1, wherein the printed circuit board has a line of bilateral symmetry which bisects the printed circuit board into a first lateral half and a second lateral half.

4. (Original) The memory module of Claim 3, wherein the first row is substantially perpendicular to the line of bilateral symmetry.

5. (Original) The memory module of Claim 4, wherein the first row is bilaterally symmetric with respect to the line of bilateral symmetry.

6. (Original) The memory module of Claim 3, wherein the second row is substantially perpendicular to the line of bilateral symmetry.

7. (Original) The memory module of Claim 6, wherein the second row is bilaterally symmetric with respect to the line of bilateral symmetry.

8. (Currently Amended) The memory module of Claim 3, wherein the ~~control logic bus comprises a~~ first set of address signal paths ~~which~~ connect the integrated circuits of the first row and the second row on the first lateral half to the first register and the ~~control logic bus comprises a~~ second set of address signal paths ~~which~~ connect the integrated circuits of the first row and the second row on the second lateral half to the second register, the first set of address signal paths and the second set of address signal paths being bilaterally symmetric to one another across the line of bilateral symmetry.

9. (Currently Amended) The memory module of Claim 1, wherein the first register addresses the identical integrated circuits located in the first row and in the second row on [[a]]the first lateral portion of the printed circuit board, and the second register addresses the identical integrated circuits located in the first row and in the second row on [[a]]the second lateral portion of the printed circuit board.

10. (Original) The memory module of Claim 9, wherein the first lateral portion comprises a first lateral half of the printed circuit board and the second lateral portion comprises a second lateral half of the printed circuit board.

11. (Currently Amended) A method of accessing data bits of a data word, the method comprising:

providing a memory module comprising:

a printed circuit board having a first lateral portion and a second lateral portion;

a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;

a control logic bus connected to the plurality of identical integrated circuits, the control logic bus comprising a first set of address signal paths connected to the integrated circuits of the first row and the second row on the first

lateral portion and a second set of address signal paths connected to the integrated circuits of the first row and the second row on the second lateral portion; and

a first register and a second register connected to the control logic bus, wherein the first register is connected to the integrated circuits of the first row and the second row on the first lateral portion by the first set of address signal paths and the second register is connected to the integrated circuits of the first row and the second row on the second lateral portion by the second set of address signal paths;

accessing a first range of data bits and a second range of data bits using the first register, the first range and the second range of data bits being first and second non-contiguous subsets of the data word; and

accessing a third range of data bits and a fourth range of data bits using the second register, the third range and the fourth range of data bits being third and fourth non-contiguous subsets of the data word.

12. (Original) The method of Claim 11, wherein:

the first range of data bits comprise data bits 0 to 15;

the second range of data bits comprise data bits 32 to 47;

the third range of data bits comprise data bits 16 to 31; and

the fourth range of data bits comprise data bits 48 to 63.

13. (Original) The method of Claim 11, wherein the printed circuit board has a line of bilateral symmetry which bisects the printed circuit board into a first lateral half and a second lateral half.

14. (Original) The method of Claim 13, wherein the first row is substantially perpendicular to the line of bilateral symmetry.

15. (Original) The method of Claim 14, wherein the first row is bilaterally symmetric with respect to the line of bilateral symmetry.

16. (Original) The method of Claim 13, wherein the second row is substantially perpendicular to the line of bilateral symmetry.

17. (Original) The method of Claim 16, wherein the second row is bilaterally symmetric with respect to the line of bilateral symmetry.

18. (Currently Amended) The method of Claim 13, wherein the ~~control logic bus comprises a~~ first set of address signal paths ~~which~~ connect the integrated circuits of the first row and the second row on the first lateral half to the first register and the ~~control logic bus comprises a~~ second set of address signal paths ~~which~~ connect the integrated circuits of the first row and the second row on the second lateral half to the second register, the first set of address signal paths and the second set of address signal paths being bilaterally symmetric to one another across the line of bilateral symmetry.

19. (Currently Amended) The method of Claim 11, wherein the first register addresses the identical integrated circuits located in the first row and in the second row on [[a]]the first lateral portion of the printed circuit board, and the second register addresses the identical integrated circuits located in the first row and in the second row on [[a]]the second lateral portion of the printed circuit board.

20. (Original) The method of Claim 19, wherein the first lateral portion comprises a first lateral half of the printed circuit board and the second lateral portion comprises a second lateral half of the printed circuit board.

21. (Cancelled)